NRJ 2124

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Dmitriy Rumynin

Title: METHOD AND DEVICE FOR PERFORMING OPERATIONS INVOLVING MULTIPLICATION OF SELECTIVELY PARTITIONED BINARY INPUTS USING BOOTH ENCODING

Docket No.: 1365.066US1
Filed: February 6, 2004
Examiner: Unknown

Serial No.: 10/774,363
Due Date: N/A
Group Art Unit: 2124

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X A Communication Concerning Related Applications (1 pg.).
X A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (4 pgs.), and copies of 41 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: _____
Atty: Timothy B Clise
Reg. No. 40,957

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JAMES KANYUSIK
Name

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Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dmitriy Rumynin	Examiner: Unknown
Serial No.:	10/774,363	Group Art Unit: 2124
Filed:	February 6, 2004	Docket: 1365.066US1
Title:	METHOD AND DEVICE FOR PERFORMING OPERATIONS INVOLVING MULTIPLICATION OF SELECTIVELY PARTITIONED BINARY INPUTS USING BOOTH ENCODING	

COMMUNICATION CONCERNING RELATED APPLICATION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
10/714408	November 14, 2003	1365.063US1	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Respectfully submitted,

DMITRIY RUMYNIN

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 16 Aug '04 By _____
Timothy B. Clise
Reg. No. 40,957

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JAMES KANYUSIK
Name

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Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dmitriy Rumynin	Examiner:	Unknown
Serial No.:	10/774,363	Group Art Unit:	2124
Filed:	February 06, 2004	Docket:	1365.066US1
Title:	METHOD AND DEVICE FOR PERFORMING OPERATIONS INVOLVING MULTIPLICATION OF SELECTIVELY PARTITIONED BINARY INPUTS USING BOOTH ENCODING		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

DMITRIY RUMYNIN

By his Representatives,

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Date 16 Aug '04

By
Timothy B Clise
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JAMES KAUKSIK
Name

Signature

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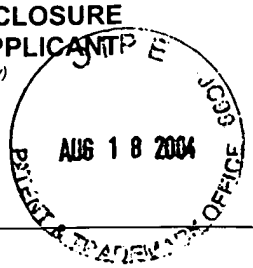

Complete if Known	
Application Number	10/774,363
Filing Date	February 6, 2004
First Named Inventor	Rumynin, Dmitriy
Group Art Unit	2124
Examiner Name	Unknown

Sheet 1 of 4

Attorney Docket No: 1365.066US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-2002/0026465	02/28/2002	Rumynin, D, et al.	708	210	01/25/2001
	US-2002/0078110	06/20/2002	Rumynin, D, et al.	708	210	07/27/2001
	US-3,634,658	01/11/1972	Brown, Richard	235	92LG	03/19/1970
	US-3,757,098	09/04/1973	Wright, Carl	235	175	05/12/1972
	US-4,399,517	08/16/1983	Niehaus, Jeffrey A., et al.	364	784	03/19/1981
	US-4,463,344	07/31/1984	Adler, R., et al.	340	347 DD	12/31/1981
	US-4,596,256	06/24/1986	Ascher, Gilles, et al.	128	710	01/26/1984
	US-4,607,176	08/19/1986	Burrows, James, et al.	307	449	08/22/1984
	US-4,993,421	02/19/1991	Thornton, William	128	670	07/20/1990
	US-5,095,457	03/10/1992	Ho-sun Jeong,	364	758	02/01/1990
	US-5,175,862	12/29/1992	Phelps, Andrew, et al.	395	800	06/11/1990
	US-5,187,679	02/16/1993	Vassiliadis, Stamatis , et al.	364	786	06/05/1991
	US-5,325,320	06/28/1994	Chiu, Chiao-Er A.	364	760	05/01/1992
	US-5,343,417	08/30/1994	Flora, Laurence P.	364	758	11/20/1992
	US-5,363,099	11/08/1994	Allen, J.	341	107	10/04/1993
	US-5,475,388	12/12/1995	Gormish, M. , et al.	341	107	10/22/1993
	US-5,497,342	03/05/1996	Mou, Z.-J., et al.	364	786	11/09/1994
	US-5,524,082	06/04/1996	Horstmann, P., et al.	364	489	06/28/1991
	US-5,712,792	01/27/1998	Yamashita, Shunzo, et al.	364	489	04/17/1996
	US-5,964,827	10/12/1999	Ngo, H. C., et al.	708	710	11/17/1997
	US-5,995,029	11/30/1999	Ryu, Myung	341	101	10/29/1997
	US-6,023,566	02/08/2000	Belkhale, K., et al.	395	500.03	04/14/1997
	US-6,173,414	01/09/2001	Zumkehr, J. , et al.	714	6	05/12/1998
	US-6,175,852	01/16/2001	Dhong, S. H., et al.	708	712	07/13/1998
	US-6,269,386	07/31/2001	Siers, S. E., et al.	708	710	10/14/1998
	US-6,490,608	12/03/2002	Zhu, Jay	708	626	12/09/1999
	US-D341,423	11/16/1993	Bible, C	D24	167	02/14/1991
	US-D377,983	02/11/1997	Sabri, M , et al.	D24	167	09/13/1995
	US-D407,159	03/23/1999	Roberg, Anne-Marie	D24	167	04/30/1998

EXAMINER **DATE CONSIDERED**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number	10/774,363
Filing Date	February 6, 2004
First Named Inventor	Rumynin, Dmitriy
Group Art Unit	2124
Examiner Name	Unknown

Sheet 2 of 4

Attorney Docket No: 1365.066US1

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]
	EP-0168650 A2	01/22/1986	Darringer, J., et al.	G06F	15/60	
	EP-0309292 A2	03/29/1989	Nishiyama, T., et al.	G06F	15/60	
	EP-0442356 A2	08/21/1991	Chang, Yen C.			
	EP-0741354 A2	11/06/1996	Ichikawa, Takeshi	G06F	7/50	
	FR-2475250 With English Abstract	08/07/1981	Houdard, Jean-Pierre , et al.	606F	7/38	
	GB-2016181	09/19/1979	Gajski, Daniel , et al.	606F	7/39	
	GB-2062310	05/20/1981	Ohhashi, Masahide , et al.	606F	7/52	
	GB-2365636	02/20/2002	Rumynin, D , et al.	G06F	7/60	
	GB-2365637	02/20/2002	Dmitriy, R	G06F	7/60	
	WO-99/22292	05/06/1999	Verbauwhede, Ingrid	G06F	7/52	
	WO-02/12995	02/14/2002	Meulemans, P	G06F	7/00	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		BEDRIJ, O. J., "Carry-Select Adder", IRE Trans., EC-11, (June 1962),340-346	
		BOOTH, ANDREW , "A Signed Binary Multiplication Technique", Oxford University Press, Reprinted from Q.J. Mech. Appl. Math. 4:236-240,(1951),Pgs. 100-104	
		CHAKRABORTY, S. , et al., "Synthesis of Symmetric Functions for Path-Delay Fault Testability", 12th International Conference on VLSI Design, (1999),pp. 512-517	
		DADDA, L. , "On Parallel Digital Multipliers", Associazione Elettrontecnia ed Elettronica Italiana, Reprinted from Alta Freq. 45:574-580, (1976),pp. 126-132	
		DADDA, L. , "Some Schemes For Parallel Multipliers", Assocciazione Elettrotenica ed Elettronica Italiana, Reprinted from Alta Freq. 34:349-356,(1965),Pgs. 118-125	
		DE MICHELI, G. , et al., "Optimal State Assignment for Finite State Machines", IEEE Transactions on Computer-Aided Design, Vol. CAD-4 (3), (July 1985),pp. 269-285	
		DEBNATH, D. , "Minimization of AND-OR-EXOR Three-Level Networks with AND Gate Sharing", IEICE Trans. Inf. & Syst., E80-D, 10, (1997),pp. 1001-1008	
		DRECHSLER, R. , et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", IEEE ED&TC 1995, Proceedings European Design and Test Conference, (March 6-9, 1995),91-97	
		FLEISHER, H , "Combinatorial Techniques for Performing Arithmetic and Logical Operations", IBM Research Center, RC-289, Research Report, (July 18, 1960),22 pages	

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Group Art Unit	2124
Examiner Name	Unknown

Sheet 3 of 4

Attorney Docket No: 1365.066US1

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		FOSTER, CAXTON , et al., "Counting Responders in an Associative Memory", The Institute of Electrical and Electronics Engineers, Inc., Reprinted, with permission, from IEEE Trans. Comput. C-20:1580-1583,(1971),Pgs. 86-89	
		GOTO, et al., "A 54 x 54-b Regularly Structured Tree Multiplier", IEEE Journal of Solid-State Circuits, Vol 27, No. 9, (Sept. 1992),1229-1236	
		HEKSTRA, et al., "A Fast Parallel Multiplier Architecture", IEEE International Symposium on Circuits and Systems; Institute of Electrical and Electronic Engineers, c1977-c1996, 20v. :ill. :28cm, (1992),2128-2131	
		HO, I. , et al., "Multiple Addition by Residue Threshold Functions and Their Representation By Array Logic", The Institute of Electrical and Electronics Engineers, Inc., Reprinted, with permission from IEEE Trans. Comput. C-22: 762-767, (1973),pp. 80-85	
		JONES, JR., ROBERT , et al., "Parallel Counter Implementation", Conf. Rec. 26th Asilomar Conf. Signals, Systems & Computers, 1, (1992),pp. 381-385	
		KNOWLES, S. , "A Family of Adders", Proc. 14th IEEE Symp. on Computer Arithmetic, (1999),30-34	
		KOC, C , "High-Speed RSA Implementation", available at ftp://ftp.rsasecurity.com/pub/pdfs/tr201.pdf., Version 2.0,(November, 1994),73 pages	
		KOC, C , "RSA Hardware Implementation", available at ftp://ftp.rsasecurity.com/pub/pdfs/tr801.pdf., Version 1.0,(August, 1995),30 pages	
		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", IEEE Trans. Computers, Vol. C-22, No. 8, (Aug. 1973),786-793	
		LADNER, RICHARD E., et al., "Parallel Prefix Computation", Journal of ACM, Vol. 27, No. 4, (Oct. 1980),831-838	
		LING, HUEY , "High-Speed Binary Adder", IBM Journal of Research and Development, Vol. 25, No. 3, (1981),156-166	
		MONTEIRO, J. , et al., "Bitwise Encoding of Finite State Machines", Proceedings of the 7th International Conference on VLSI Design, (Jan. 1994),pp. 379-382	
		NIENHAUS, H. , "Efficient Multiplexer Realizations of Symmetric Functions", IEEE, (1981),pp. 522-525	
		OKLOBDZIJA, V G., et al., "Improving multiplier design by using improved column compression tree and optimized final adder in CMOS technology", IEEE transactions on Very Large Scale Integration (VLSI) Systems, IEEE, Inc, New York, vol. 3, no. 2,(1995),292-301	
		SKLANSKY, J. , "Conditional-Sum Addition Logic", IRE Trans., EC-9, (June 1960),226-231	
		SWARTZLANDER JR., E E., "Parallel Counters", IEEE Transactions on Computers, C-22(11), (November 1973),1021-1024	

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Sheet 4 of 4

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		VASSILIADIS, S. , et al., "7/2 Counters and Multiplication with Threshold Logic", IEEE, (1997),pp. 192-196	
		VILLA, TIZIANO , et al., "NOVA: State Assignment of Finite State Machines for Optimal Two-Level Logic Implementation", IEEE Transactions on Computer-Aided Design, Vol. 9, No. 9,(September 1990),905-924	
		WALLACE, C. , "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, Vol. EC-13,(1964),pp. 14-17	
		WEINBERGER, A. , et al., "A Logic for High-Speed Addition", Nat. Bur. Stand. Circ., 591, (1958),3-12	
		ZURAS, D , et al., "Balanced delay trees and combinatorial division in VLSI", IEEE Journal of Solid State Circuits, SC-21, IEEE Inc, New York, Vol. SC-21, no. 5,(1986),814-819	

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